PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
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Serial No.: 10/664,665

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For: METHOD FOR DETERMINING THE RELIABILITY OF DIELECTRIC LAYERS

Confirmation No.: 4618

Examiner: Laura M. Schillinger

Group Art Unit: 2813

Att'y Docket: 2000.111200/H2022

Customer No.: 23720

APPEAL BRIEF

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby submit this Appeal Brief to the Board of Patent Appeals and Interferences in response to the Final Office Action dated August 24, 2006. The Notice of Appeal was filed on October 20, 2006.

The Director is authorized to deduct the fee for filing this Appeal Brief ($500), or any additional fees under 37 C.F.R. §§ 1.16 to 1.21 required for any reason relating to this document, from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.111200.

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Applicants are not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1-18 are pending in the application. Claims 1-76 were originally filed with the application. Claims 19-76 were canceled in Applicants' Response to Office Action Dated February 8, 2005 (mailed April 19, 2005) because they were subject to a previous restriction requirement dated November 8, 2004. Claims 77-84 were added in Applicants' Response to Office Action Dated February 8, 2005. Claims 77-84 were withdrawn from consideration by the Examiner in the Final Office Action dated July 12, 2005. Claims 1-16 and 18 are at issue in this appeal and they are attached as Appendix A. Claims 1-16 and 18 were rejected (claim 17 was objected to) in the Final Office Action issued on August 24, 2006. Claims 1-16 and 18 are the subject of the present appeal.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In general, the present invention is directed to semiconductor fabrication technology, and, more particularly, to a method of assessing the reliability of dielectric layers formed as part of, for example, semiconductor devices. There is one independent claim at issue in the current appeal: claim 1.

Independent claim 1 is generally directed to a method including providing a device 40 having a dielectric layer 44, applying a plurality of constant voltage pulses to the device 40, wherein each of the voltage pulses are at the same voltage level, and determining a time-to-breakdown for the dielectric layer 44 based upon a count of the number of pulses applied to the device 40 to break down the dielectric layer 44. By way of example only, at least portions of the invention are described at p. 10, ll. 1-12, p. 11, l. 13 – p. 14, l. 14, and Figures 2-4.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-16 and 18 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lin (U.S. Patent No. 6,602,729) in view of Niino (U.S. Patent No. 5,433,790).

VII. ARGUMENT

A. Legal Standards

As the Board well knows, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. Moreover, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). If an independent claim is nonobvious

under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988); M.P.E.P. § 2143.03.

With respect to alleged obviousness, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Health-care Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. The consistent criterion for determining obviousness is whether the prior art would have suggested to one of ordinary skill in the art that the process should be carried out and would have a reasonable likelihood of success, viewed in the light of the prior art. Both the suggestion and the expectation of success must be founded in the prior art, not in the Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991; *In re O'Farrell*, 853 F.2d 894 (Fed. Cir. 1988); M.P.E.P. § 2142.

B. The Examiner Erred in Rejecting Claims 1-16 and 18

All of these claims were rejected under 35 U.S.C. § 103 based upon Lin and Niino. It is respectfully submitted that the Examiner erred in rejecting these claims as the rejections are based upon misunderstandings of the claimed invention and the cited prior art, and because the rejections reflect an improper use of hindsight using Applicants' disclosure as a roadmap. A recent Federal Circuit case makes it crystal clear that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61

U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35. "Our case law makes clear that the best defense against the subtle but powerful attraction of hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." *Telefex v. KSR Intern. Co.*, 119 Fed. Appx. 282 (Fed. Cir. 2005) (unpublished) (citations omitted).

1. Independent Claim 1 is Allowable

It is believed that the Examiner's rejection of independent claim 1 is based upon a misunderstanding of the claimed invention. In general, the present invention is directed to a method that includes, among other things, applying a plurality of constant voltage pulses to the device recited in claim 1. That is, for example, a plurality of pulses – each of which have the same constant voltage – are applied to the device. In addition to requiring the plurality of constant voltage pulses (each of which are at the same voltage level), claim 1 recites that the step of determining a time-to-breakdown for the dielectric layer based upon a count of the number of pulses applied to the device to break down the dielectric layer. It is respectfully submitted that the combination of Lin and Niino does not disclose nor suggest the method set forth in independent claim 1.

In the Final Office Action (p. 3), the Examiner concedes that Lin does not disclose the claimed limitation "wherein each of the voltage pulses are at the same voltage level." The Examiner then cites to Niino for the concept that Niino teaches "a voltage pulse at the same voltage level as claimed by the Applicant." Final office Action, p. 3. In doing so, the Examiner erred.

Niino is directed to an allegedly improved device for forming or depositing films on semiconductor devices. Abstract; Col. 1, ll. 10-18; Col. 4, ll. 21-32. The portions of Niino cited by the Examiner in support of the rejection, col. 11, ll. 15-25, is directed to the voltage applied to deposit a layer of material – the voltage levels discussed in Niino have nothing to do with determining the reliability of dielectric layers. Respectfully, this demonstrates that the Examiner merely sought out bits and pieces of the claimed invention from various prior art sources and, in conclusory fashion, stated that such a combination would have been obvious to one skilled in the art. It is unclear to the undersigned why anyone skilled in the art, when addressing the issue of assessing the reliability of dielectric layers, would be motivated to look at Niino – a reference that is directed to an allegedly unique device for depositing layers of material – a reference that says absolutely nothing about determining the reliability of a dielectric layer. It is believed that the Examiner's rejection reflects an improper use of hindsight using Applicants' disclosure as a road map. The Examiner's rejection should be reversed for at least this reason.

Additionally, the Examiner's rejection reflects a fundamental misunderstanding of another aspect of the claimed invention as well as the disclosure of Lin. The Examiner cites to col. 3, ll. 1-5, of Lin for support that Lin discloses determining breakdown based on a count of the number of pulses. Final Office Action, p. 3 (emphasis added). Applicants respectfully disagree.

Lin is understood to be directed to a method of testing a dielectric material. Abstract. To that end, Lin proposes use of a testing methodology wherein a reference current (I_{ref}) is initially established. This reference current is chosen to be a value below the breakdown current (I_{bd}) of the dielectric layer but greater than the expected base current so as to avoid wasting time on unnecessary early measurements of the base current. According to Lin, Figure 2 disclosed

therein is a flowchart of a prior art method of testing dielectric layers. Lin specifically notes that the stress voltage (V_s) may be incremented at node 4 and the loop disclosed therein may continue. Lin goes on to set forth a flowchart (Figure 5) for the invention described therein. Lin specifically notes that if the measured stress current (I_s) is the same or lower than the reference current (I_{ref}), then the stress voltage is incremented by an amount and the procedure continues through the testing loop. Col. 3, ll. 38-52. As understood by the undersigned, the methodology disclosed in Lin involves incrementally increasing the voltage applied to the dielectric layer until breakdown occurs. Col. 2, ll. 53-56; Col. 3, ll. 14-17; Col. 3, ll. 49-52. Moreover, the methodologies disclosed in Lin for determining the breakdown of the dielectric layer involve measuring and detecting the breakdown current (I_{bd}) – **NOT COUNTING THE NUMBER OF PULSES**. Figure 3; Col. 3, ll. 18-25.

As thus understood, it is clear that the Examiner erred in rejecting claim 1. As set forth above, Lin does not disclose applying a plurality of constant voltage pulses. Moreover, Lin does not disclose or suggest a method wherein the time-to-breakdown of a dielectric layer determined based upon a count of the number of pulses applied to break down the dielectric layer. Lin specifically discloses a methodology whereby the applied voltage is incremented or increased at each successive step until breakdown occurs. At no point is the concept of applying constant voltage pulses and determining breakdown based upon the a count of the number of those applied pulses even remotely disclosed or suggested in Lin.

For at least the aforementioned reasons, it is clear that the Examiner erred in rejecting independent claim 1, and all claims depending therefrom. Accordingly, the Examiner's rejection should be REVERSED.

2. Dependent Claims 2 and 3 Are Allowable

It is further submitted that the Examiner erred in rejecting dependent claims 2 and 3, as they are allowable over the art of record for reasons independent of those set forth above with respect to independent claim 1. According to these dependent claims, the invention set forth in claim 1 further comprises measuring a current through the dielectric layer after one or more or each (depending upon the claim) of the plurality of constant voltage pulses has been applied. Lin simply does not disclose or suggest a methodology of measuring a current after the application of one or more constant voltage pulses. Accordingly, dependent claims 2 and 3 are likewise believed to be allowable independent of their dependence upon claim 1.

For at least the aforementioned reasons, it is clear that the Examiner erred in rejecting dependent claims 2 and 3. Accordingly, the Examiner's rejection should be REVERSED.

3. Dependent Claim 14 Is Allowable

The Examiner also erred in rejecting dependent claim 14. Dependent claim 14 is allowable for reasons other than its dependency upon independent claim 1. In rejecting claim 14, the Examiner cited to Col. 3, ll. 8-17, of Lin. Final Office Action, p. 5. Applicants respectfully disagree. Claim 14 involves the step of determining at least one parameter of a process operation to be performed to form a dielectric layer on at least one subsequently processed substrate based upon the determined time-to-breakdown. The passages of Lin identified by the Examiner simply do not address or even mention this aspect of the currently claimed invention, as recited in claim 14. The identified passages of Lin merely describe a prior art methodology wherein stress currents (I_s) and base currents (I_b) are measured and wherein the stress voltage may be incremented if breakdown has not yet occurred. There is simply no suggestion in Lin, or any other art of record, for determining at least one parameter of a process operation to be performed

to form a dielectric layer on at least one subsequently processed substrate based upon the determined time-to-breakdown. Accordingly, it is respectfully submitted that dependent claim 14 is independently allowable over the art of record.

For at least the aforementioned reasons, it is clear that the Examiner erred in rejecting dependent claim 14. Accordingly, the Examiner's rejection should be REVERSED.

VIII. CLAIMS APPENDIX

The claims that are the subject of the present appeal – claims 1-16 and 18 – are set forth in the attached "Claims Appendix."

IX. EVIDENCE APPENDIX

Applicants do not rely upon any evidence as indicated on the attached Evidence Appendix.

X. RELATED PROCEEDINGS APPENDIX

There are no Related Proceedings for this appeal as indicated on the attached Related Proceedings Appendix.

XI. CONCLUSION

It is respectfully submitted that the Examiner's obviousness rejections are based on fundamental misunderstandings of the claimed inventions and the prior art and also reflect an improper use of hindsight using Applicants' disclosure as a roadmap. A recent Federal Circuit case makes it crystal clear that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir.

2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35. "Our case law makes clear that the best defense against the subtle but powerful attraction of hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." *Telefex v. KSR Intern. Co.*, 119 Fed. Appx. 282 (Fed. Cir. 2005) (unpublished) (citations omitted).

Accordingly, it is respectfully submitted that the Examiner erred in not allowing claims 1-16 and 18 over the prior art of record. Applicants respectfully request the Board **REVERSE** the Examiner's rejections. The undersigned attorney may be contacted at (713) 934-4055 with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,

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Date: December 11, 2006

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CLAIMS APPENDIX

1. A method, comprising:

providing a device having a dielectric layer;

applying a plurality of constant voltage pulses to said device, wherein each of said voltage pulses are at the same voltage level; and

determining a time-to-breakdown for said dielectric layer based upon a count of the number of pulses applied to said device to break down said dielectric layer.

2. The method of claim 1, further comprising measuring a current through said dielectric layer after one or more of said constant voltage pulses has been applied.

3. The method of claim 1, further comprising measuring a current through said dielectric layer after each of said plurality of constant voltage pulses has been applied.

4. The method of claim 1, wherein said time-to-breakdown is determined based upon a measurement of current flowing through said dielectric layer, said current being measured after one or more of said constant voltage pulses has been applied.

5. The method of claim 1, wherein said device is comprised of at least one of a transistor, a capacitor, a resistor and a memory cell.

6. The method of claim 1, wherein said dielectric layer is comprised of silicon dioxide or a material having a dielectric constant greater than 5.

7. The method of claim 1, wherein said constant voltage pulses have a voltage that ranges from approximately 4-5 volts.

8. The method of claim 1, wherein said pulses have a constant pulse width.

9. The method of claim 1, wherein said pulses have a constant pulse width of less than 1 μsec.

10. The method of claim 1, wherein said pulses have a constant pulse width of approximately 100 ns.

11. The method of claim 2 or 3, wherein said step of measuring said current through said dielectric layer is performed using an applied voltage of approximately 1-2 volts.

12. The method of claim 1, wherein said device is a transistor and said dielectric layer is a gate insulation layer for said transistor.

13. The method of claim 1, wherein said dielectric layer is an interlevel or intralevel dielectric layer of a conductive interconnection structure.

14. The method of claim 1, further comprising:

determining at least one parameter of a process operation to be performed to form a dielectric layer on at least one subsequently processed substrate based upon said determined time-to-breakdown.

15. The method of claim 14, further comprising:

performing said process operation comprised of said determined at least one parameter on said at least one subsequently processed substrate to form said dielectric layer above said at least one subsequently processed substrate.

16. The method of claim 14, wherein determining said at least one parameter comprises determining at least one of a temperature, a pressure, a duration, a process gas composition, a process gas concentration, and an applied voltage of said at least one process operation.

17. The method of claim 14, wherein said at least one process operation comprises at least one of a deposition process, a thermal growth process and a nitridation process.

18. The method of claim 1, wherein said device is part of a test structure formed on a semiconducting substrate.

EVIDENCE APPENDIX

Applicants do not rely on any evidence for this appeal.

RELATED PROCEEDINGS APPENDIX

There are no Related Proceedings for this appeal.